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A General Cost-effective Design Structure for Probabilistic-Based Noise-Tolerant Logic Functionsin Nanometer CMOS Technology

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Abstract—Noise-immunity of a logic gate or a circuit is now an important design criterion with dimension scaling to nanometers. Two noise-immune design structures based on *Markov random field* (MRF) have been proposed in [1], [2] and [3]. These design structures can achieve an excellent noise-immunity but with a large number of redundant transistors. In this paper, a general noise-immune design structure easy to implement has been proposed. It can achieve nearly the same noise-immunity as *Master-and-Slave* MRF (MAS MRF) [3] but with a significantly less area penalty. Basic logic gates are simulated and comparison of different circuits based on different design structures is presented. These simulations are based on the *Berkeley Predictive Technology Model* (BPTM) 65nm CMOS Technology [4] and ST 65nm CMOS models.

Index Terms—*Markov random field* (MRF), noise-immunity, general cost-effective structure, CMOS

INTRODUCTION

The CMOS dimension scaling technology has dramatically improved the performances of transistors and devices in the past decades. In order to keep the power dissipation constant or at a low degree, the supply voltage should scale linearly with the size [5]. In this situation, the reduction of noise margin makes the transistors and devices working in a noisy signal environment. As a result, the transistors in nanometers are much more prone to soft errors, and thus the noise-immune ability of a logic gate or a circuit becomes an important designcriterion [6].

For the intrinsic random nature of noise, traditional fault- tolerant design methodologies based on hardware redundancy,
e.g. Triple-Modular-Redundancy (TMR) [7], Cascade TMR (CTMR) [8], are not capable to obtain noise-immunity. The noise interferes the input signal of each module and de- grades the right judgment of the majority voter. The NAND- multiplexing methodology proposed by Von Neumann [9] can produce the reliable result using unreliable components. However, it needs an extremely high degree of redundancy [10]. The reconfiguration technology is more effective to deal with manufacturing defects or permanent faults and requires enormous amounts of redundancy [11].

Therefore, the traditional approaches are not effective to attain noise-immunity for the random and dynamic nature of noise. Probabilistic-based technologies are more suitable to

deal with this problem [12], [13], [14]. One of the promising noise-tolerant probabilistic-based designs is proposed in [1], which is based on *Markov random field* (MRF) [15]. Accord- ing to Nepal *et al.* [1], the reliability or the noise-immunity of a circuit can be improved by maximizing the joint probability of valid input-output pairs with a cost of hardware redundancy. Furthermore, it was optimized in [2] in order to reduce its areapenalty. In [3], a *Master-and-Slave* MRF (MAS MRF) design structure was proposed by Wey *et al.*, which can obtain nearly the same noise-immune ability as structures in [1], [2] but withfewer transistors. In addition to the area over-cost, another disadvantage of approaches proposed in [1], [2], [3] is that they did not propose a general design structure applicable to all the basic logic gates. In other words, we should design every single logic gate specially. Also another approach based on MRF was proposed in [16], which is based on *Differential Cascode Voltage Switch* (DCVS). However, this methodology is just desirable for an inverter.

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In this work, we propose a general cost-effective noise-immune design structure of logic functions. Compared with MAS MRF structure, our proposed structure can be imple- mented to all the basic logic gates with nearly the same noise- immune ability and a much less area cost. Furthermore, this generality means that the proposed structure applies also for functions involving several logic gates and is therefor much more cost effective than the solutions mentioned before.

This paper is organized as follows. Section II reviews the preliminaries on MRF theory and the previous noise-immune circuit design structures. The proposed design structure is described in Section III. Section IV shows the simulation results and comparisons of different design structures. Simula- tions have been done in SPICE using the *Berkeley Predictive Technology Model* (BPTM) 65nm CMOS Technology [4] and in Spectre based on ST 65nm CMOS models. Finally, discussions and conclusions are given in Section V.

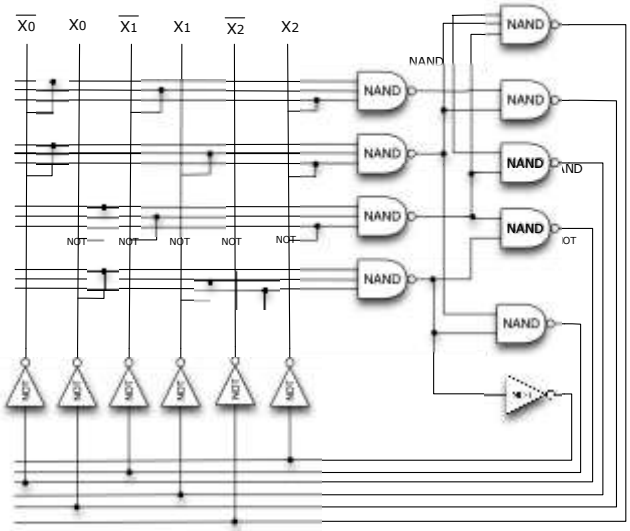

Fig. 3. The two-input MRF NAND gate implementation. The two inputs are
$\square_0$ and $\square_1$, the output is $\square_2$.

According to the Boolean simplification and valid

which can be defined either continuous or discrete according to

For example, for a MAS MRF NAND logic gate, the minterms with $\square_2$ belong to group "1" and the minterms with

— $\square_2$ belong to group "0". It reduces the valid states generator
from four NAND gates in Fig. 3 to one NAND gate, one NOR gate plus two inverters. As for the feedback loop, it contains only two NAND gates and two inverters while in Fig. 3, five NAND gates and seven inverters are required. The MAS MRF NAND gate is presented in Fig. 5.

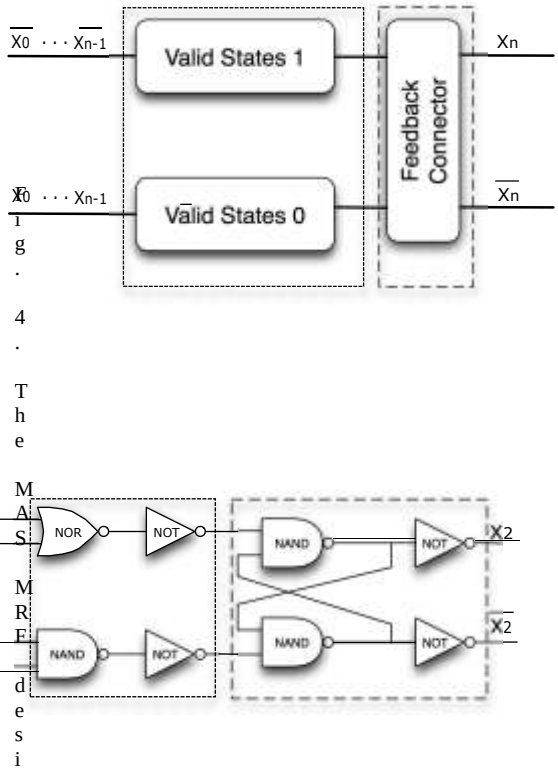

Fig. 4. The MAS MRF NAND gate implementation.

minterms reduction, an optimized expression of equation (6) is given as:

Fig. 5. The two-input MAS MRF NAND gate implementation.

I. PROPOSED GENERAL LOGIC GATES DESIGN STRUCTURE

We propose a general **C**ost-**E**ffective **N**oise-**T**olerant circuit

$$E(x_0, x_1, x_2) = -\sum_{x} x_i(x_0, x_1, x_2)$$
$$= -(\overline{x_0}\,x_1\overline{x_2} + x_0\overline{x_1}\,x_2 + x_0x_1\overline{x_2} + x_0x_1x_2)$$
$$= -((x_0 + \overline{x_1})x_2 + (x_0x_1)\overline{x_2}) \quad (7)$$

According to equation (7), Nepal *et al*. optimized the generation of the valid states and thus reduced the transistor numbers, as proposed in [2].

Another design structure is MAS MRF [3]. Its structure is shown in Fig. 4. The *Master* subset generates the valid states and the *Slave* subset is the feedback loop. The *Master* subset divides the valid states into the valid groups "0" and "1". All the valid states with the output value 1 compose the "1" group and those with output value 0 compose "0" group. Compared with [1], another advantage of MAS MRF is the redesign of the feedback loop, which reduces the transistor number and the hardware complexity.

design structure based on **M**arkov **R**andom **F**ield, named CENT MRF. In order to illustrate the proposed approach, takeaccount of the NAND gate. Its corresponding energy function is given in equation (7). We know that

where $x_{\square\square\square\square}(x_0, x_1)$ is the logic function of a NAND gate. Its input signals are x_0, x_1 and its output signal is x_2.

We propose to proceed in the same way to obtain the energyfunction of any logic gate. Especially, this produces the energy function for the basic logic gates as shown bellow.

A. Simulation results (SPECTRE)

Spectre simulator has been used for simulations of basic logic gates as well as more complex logic combinational func- tions such as a one-bit full-adder (FA), a four-bit Ripple CarryAdder (RCA) and a (8, 4) Hamming Decoder to compare the noise-immunity of different design structures. We used the low threshold voltage and low power PMOS (plvtlp) and NMOS (nlvtlp) transistors of ST 65nm library. The supply voltage of the gates is $1.2\square$ and the temperature is $25^{\circ}\square$. Different input signals with different *signal-noise-ratio* (SNR) were simulated and KLDs of output signal were quantified. If there were more than one output in the circuit, the output signal of *deepest-path*was treated as the representation.

The simulation results are shown in Fig. 10 to Fig. 14. TableII shows the comparison of the transistor number for different bench circuits.

II. DISCUSSIONS AND CONCLUSIONS

This paper proposed a general cost-effective noise-tolerant circuit structure based on Markov Random Field. It is a generaldesign approach easy to implement for all logic combinational

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